# APPLICATION FOR UNITED STATES LETTERS PATENT

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TITLE: FLOATING-BODY RANDOM DYNAMIC ACCESS MEMORY WITH PURGE LINE

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# FLOATING-BODY DYNAMIC RANDOM ACCESS MEMORY WITH PURGE LINE

## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

[1] The field of invention generally relates to electronics.

### 2. Background of the Related Art

[2] Electronics are very important to the lives of many people. In fact, electronics are present in almost all electrical devices (e.g. radios, televisions, toasters, and computers). It may be desirable for electronics to be designed as small as possible. Also, it may be desirable for electronics to operate as fast as possible. In fact, in some circumstances, electronics will operate faster when they are made smaller. Smaller devices may consume less power. Electronics that consume less power may also generate less heat. Electronics that generate less heat may operate at faster speeds. The speed of a electronic device may be a critical attribute governing its usefulness. For example, a computer which operates at a fast speed may be able to perform many different types of tasks (e.g. displaying moving video, making complex computations, and communicating with other devices) which a relatively slow computer may not be able to perform.

## BRIEF DESCRIPTION OF THE DRAWINGS

[3] Figure 1 is an exemplary global diagram of a portion of a computer.

[4] Figure 2 is an exemplary diagram illustrating a plurality of memory cells each coupled to a bit line and a word line.

[5] Figures 3A and 3B are exemplary illustrations of a memory cell coupled to a word line and a bit line.

[6] Figure 4 is an exemplary table illustrating voltages during operation of a memory cell.

[7] Figure 5 is an exemplary illustration of a plurality of memory cells each coupled to a bit line, a word line, and a purge line.

[8] Figures 6A and 6B are exemplary illustrations of a memory cell coupled to a word line, a bit line, and a purge line.

[9] Figure 7 is an exemplary table illustrating voltages applied during operation of a memory cell.

## DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[10] Electrical hardware (e.g. a computer) may include many electrical devices. In fact, a computer may include millions of electrical devices (e.g. transistors, resistors, and capacitors). These electrical devices may work together in order for hardware to operate correctly. Accordingly, electrical devices of hardware may be electrically coupled together. This coupling may be either direct coupling (e.g. direct electrical connection) or indirect coupling (e.g. electrical communication through a series of components).

[11] Figure 1 is an exemplary global illustration of a computer. The computer may include a processor 4, which acts as a brain of the computer. Processor 4 may be formed on a die. Processor 4 may include an Arithmetic Logic Unit (ALU) 8 and may be included on the same die as processor 4. ALU 8 may be able to perform continuous calculations in order

for processor 4 to operate. Processor 4 may include cache memory 6 which may be for temporarily storing information. Cache memory 6 may be included on the same die as processor 4. Information stored in cache memory 6 may be readily available to ALU 8 for performing calculations. A computer may also include an external cache memory 2 to supplement internal cache memory 6. Power supply 7 may be provided to supply energy to processor 4 and other components of a computer. A computer may include a chip set 12 coupled to processor 4. Chip set 12 may intermediately couple processor 4 to other components of the computer (e.g. graphical interface 10, Random Access Memory (RAM) 14, and/or a network interface 16). One exemplary purpose of chip set 12 is to manage communication between processor 4 and these other components. For example, graphical interface 10, RAM 14, and/or network interface 16 may be coupled to chip set 12.

[12] Figure 2 is an exemplary diagram illustrating a plurality of memory cells ($C_{AA}$, $C_{AB}$, $C_{AC}$, $C_{BA}$, $C_{BB}$, $C_{BC}$, $C_{CA}$, $C_{CB}$, and $C_{CC}$). Each memory cell may be coupled to a bit line ($BL_A$, $BL_B$, or $BL_C$) and a word line ($WL_A$, $WL_B$, or $WL_C$). Word lines ($WL_A$, $WL_B$, and $WL_C$) may be used to activate a given memory cell. Bit lines may be used to read or write information from a given memory cell. In the exemplary illustration of Figure 2, word line $WL_A$ is used to activate cells $C_{AA}$, $C_{AB}$, and $C_{AC}$. Cells $C_{AA}$, $C_{AB}$, and $C_{AC}$ may be activated at the same time by word line $WL_A$. When cells $C_{AA}$, $C_{AB}$, or $C_{AC}$ are activated, data may be written to each of these cells through bit line $BL_A$, $BL_B$, or $BL_C$. Data stored in cells $C_{AA}$, $C_{AB}$, and $C_{AC}$ may constitute a "word", which may be activated by word line $WL_A$. A "word" may be defined as a multi-bit segment of data. Likewise, cells $C_{BA}$, $C_{BB}$, and $C_{BC}$ may be activated by word line $WL_B$. Data written to or read from cells $C_{BA}$, $C_{BB}$, and $C_{BC}$

may be communicated through bit lines $BL_A$, $BL_B$, and $BL_C$. In embodiments of the present invention, only one of word lines $WL_A$, $WL_B$, and $WL_C$ is activated at the same time, since bit lines $BL_A$, $BL_B$, and $BL_C$ are shared by the different sets of cells that constitute a word.

[13] The memory cells illustrated in Figure 2 may have one of several configurations. For example, the memory cell may be a six transistor Static Random Access Memory (SRAM) cell. Alternatively, a memory cell may be a one transistor, one capacitor Dynamic Random Access Memory (DRAM) cell. Further, in embodiments, each memory cell may be Floating Body Dynamic Random Access Memory (FBDRAM) cell. One of ordinary skill in the art would appreciate that Figure 2 merely illustrates an arbitrary number of cells in a matrix and that different dimension of such a matrix may be utilized with a corresponding number of bit lines and word lines.

[14] Figure 3A is an exemplary illustration of a memory cell which is a Floating Body Dynamic Random Access Memory (FBDRAM) cell. The cell may include a single transistor 19 connected to word line WL and bit line BL. Gate 24 of transistor 19 may be connected to word line WL. First channel interface 22 of transistor 19 may be connected to bit line BL. Second channel interface 18 of transistor 19 may be connected to ground 26. Body 20 of transistor 19 may be floating. Body 20 may be floating by being substantially electrically isolated from first channel interface 22, second channel interface 18, and gate 24. In embodiments of the present invention, first channel interface 22 may be either source or drain of transistor 19. Likewise, second channel interface 18 may be either source or drain of transistor 19. In embodiments of the present invention, transistor 19 is a MOSFET transistor.

[15] A logical 1 may be written to transistor 19 by word line WL transmitting a high voltage to gate 24 of transistor 19 and bit line BL transmitting a high voltage to first channel interface 22 of transistor 19. By this combination of voltages applied to transistor 19, an electrical charge may be collected in the floating body 20 of transistor 19. To write a logical 0 to transistor 19, a high voltage may be applied to gate 24 through word line WL and a very low voltage (e.g. negative voltage) may be applied to first channel interface 22. When a very low voltage is applied to the channel interface 22, any charges in the floating body 20 are discharged.

[16] Figure 3B is an exemplary illustration showing intrinsic features of transistor 19. Specifically, floating body 20 is illustrated as being connected to bit line BL through diode 28 and current source 30. Diode 28 and current source 30 are shown as being connected and in parallel. Diode 28 and current source 30 are not separate devices from transistor 19, but rather represent intrinsic properties of transistor 19. Although floating body 20 is theoretically electrically isolated from the other portions of transistor 19, practically, there is some electrical communication between floating body 20 and first channel interface 22.

[17] Referring to Figure 3B, when an appropriately high voltage is applied to first channel interface 22 and a high voltage is applied to gate 24, an impact ionization current flows through floating body 20. This current is represented by intrinsic current source 30. As a result of an impact ionization current, electron holes are created in the floating body 20, which effectively stores a charge in floating body 20. Likewise, when a sufficiently low voltage is applied to first channel interface 22 and a high voltage is applied to gate 24,

intrinsic diode 28 becomes forward biased and electrons migrate from floating body 20 to bit line BL, removing electron holes from floating body 20. In other words, electric charge is dissipated from the floating body when a sufficiently low voltage is applied to first channel interface 22 and a high voltage is applied to gate 24. Accordingly, when a sufficiently low voltage is applied to first channel interface 22 through bit line BL, charge is removed from floating body 20 and data stored in floating body 20 may represent a logical 0. One of ordinary skill in the art would appreciate that diode 28 and current source 30 are intrinsic attributes of transistor 19 and are not separate semiconductor structures from transistor 19.

[18] Figure 4 is an exemplary table illustrating the necessary voltage levels for operation of a floating body dynamic random access memory cell. In order to write a logical 0 or write a logical 1, a low voltage must be applied to second channel interface 18. In exemplary illustrations Figures 3A and 3B, a low voltage applied to second channel interface 18 is 0 V by being connected to ground 26. In a hold operation, a very low voltage is applied to gate 24 while a low voltage is applied to first channel interface 22. In other words, during a hold operation, the very low voltage applied to gate 24 can effectuate electrical isolation of floating body 20, so that floating body 20 can hold charges representing either a logical 0 or a logical 1.

[19] Although first channel interface 22 may ideally apply a low voltage during a hold operation, it is possible that a high voltage may be applied. As illustrated in Figure 2, bit lines $BL_A$, $BL_B$, or $BL_C$ each may service a set of cells, wherein each set of cells is in a different word. For example, in Figure 2, bit line $BL_A$ services cell $C_{AA}$, $C_{BA}$, and $C_{CA}$. During normal operation of a memory cell matrix, the bit line voltage may vary during the

hold operation, because each bit line is servicing different words. As illustrated in exemplary Figure 2, a given word line will service a plurality of cells in the same word. For example, word line $WL_A$ services cell $C_{AA}$, $C_{AB}$, and $C_{AC}$. Accordingly, cells $C_{AA}$, $C_{AB}$, and $C_{AC}$ will all have a very low voltage applied to their gates during a hold operation. In other words, an entire word will experience a hold operation at the same time. The very low voltage applied to the gates during a hold operation may insulate the charge (representing a logical 0 or logical 1) in the floating bodies from any voltage fluctuations on the bit lines.

[20] As discussed above and as shown in exemplary Figure 4, during the writing of a logical 0, the word line will apply a high voltage to gate 24 and a very low voltage on bit line BL to first channel interface 22. Likewise, during the writing of a logical 1 to transistor 19, the word line applies a high voltage to gate 24 and a high voltage on bit line BL to first channel interface 22.

[21] In certain small-scale electronic devices, it is desirable for transistors to have very small dimensions. Accordingly, voltage tolerances on interfaces of a transistor may be relatively low. When there are relatively low tolerances, the voltage difference between a gate and each channel interface cannot exceed a threshold specific to that transistor. For example, if a very low voltage is applied to gate 24 and a high voltage is applied to a first channel interface 22, breakdown may occur and the transistor will not operate. If a transistor does not operate, it will not function in a memory device.

[22] Large voltage differences which may cause breakdown are illustrated in exemplary Figure 4. During a writing of a logical 0, a high voltage is applied on word line WL to gate 24 and very low voltage is applied on bit line BL to first channel interface 22. In

this circumstance, in small-scale devices, breakdown may occur and transistor 19 may not operate properly because transistor 19 cannot tolerate the voltage difference between gate 24 (high voltage) and first channel interface 22 (very low voltage). Similarly, in a hold operation, a very low voltage is applied on the word line WL to gate 24 and the voltage level applied on bit line BL to first channel interface 22 may be either very low, low, or high. This fluctuation may be attributed to the possibility that the bit line BL services other memory cells in other words. When a write operation is implemented in another cell, a high voltage may be applied on bit line BL, which is consequently applied to first channel interface 22 of transistor 19 in the hold state. Accordingly, during a hold operation there may be a very low voltage applied to gate 24 and a high voltage applied to first channel interface 22. In small-scale electronic devices, this large voltage difference may cause breakdown and the transistor may not function.

[23] Figure 5 is an exemplary illustration of embodiments of the present invention. In embodiments, a matrix of memory cells include cells $C_{AA}$, $C_{AB}$, $C_{AC}$, $C_{BA}$, $C_{BB}$, $C_{BC}$, $C_{CA}$, $C_{CB}$, and $C_{CC}$. Each of these cells are connected to a bit line, a word line, and a purge line. For example, cell $C_{AA}$ is connected to word line $WL_A$, bit line $BL_A$ and purge line $PL_A$. Similar to Figure 2, word line $WL_A$ services a word including cells $C_{AA}$, $C_{AB}$, and $C_{AC}$. Additionally, purge line $PL_A$ services this same word.

[24] Figure 6A illustrates embodiments of the present invention including a floating body dynamic random access memory (FBDRAM) with a purge line. In these embodiments, word line WL is connected to gate 40. Bit line BL is connected to first channel interface 42. Purge line PL is connected to second channel interface 44. Floating

body 46 is substantially electrically isolated from the other components of transistor 41. In embodiments of the present invention, transistor 41 is a MOSFET transistor.

[25] In operation of transistor 41 as a memory cell, according to embodiments of the present invention, every time data is written to transistor 41, two operations must occur. First, transistor 41 must be purged of any stored electrical charges. Second, transistor 41 must be programmed according to data transmitted on bit line BL. During the purge operation, a very low voltage is applied on purge line PL to transistor 41 by applying a very low voltage to second channel interface 44. As shown in Figure 6B, intrinsic diode 48 becomes forward biased during the purge operation, consequently removing any electron holes that were previously in floating body 46. In embodiments of the present invention during the purge operation, a very low voltage may be applied to gate 40. By applying a very low voltage to gate 40, efficiency and power consumption may be improved. However, it is not absolutely necessary for a very low voltage to be applied to gate 40 in order for the purge operation to be successful.

[26] During a write operation, a low voltage may be applied to second channel interface 44 through purge line PL and a high voltage may be applied on word line WL to gate 40. If a logical 0 is written to transistor 41, a low voltage may be applied on bit line BL to first channel interface 42. In embodiments, the low voltage applied on bit line BL to transistor 41 effectively maintains a zero charge state of the floating body 46 of transistor 41. Accordingly, after the purge operation, floating body 46 may store a charge representing a logical 0. By applying low voltage on bit line BL, this charge representing a logical 0 may be maintained.

[27] During a write operation of a logical 1 to transistor 41, a high voltage is applied on bit line BL to first channel interface 42. When this high voltage is applied to first channel interface 42, an impact ionization current is applied to floating body 46, creating electron holes in the floating body and effectively storing a charge in floating body 46. The impact ionization current phenomenon is represented by intrinsic current source 50 in Figure 6B. In embodiments, intrinsic diode 48 may only be forward-biased during the purge operation and operates only when a very low voltage is applied on purge line PL to second channel interface 44. Likewise, intrinsic current source 50 may only operate during the writing of a logical 1 when a high voltage is applied on the bit line BL to first channel interface 42. In embodiments, a high voltage may be applied to gate 40 during writing of a logical 1.

[28] Figure 7 is an exemplary table illustrating voltages applied during a hold operation, a purge operation, a write logical 0 operation, and a write logical 1 operation of a floating body dynamic random access memory cell with a purge line according to embodiments of the present invention. During a hold operation, second channel interface 44 and gate 40 receive a low voltage level (e.g. ground). During a purge operation, second channel interface 44 and gate 40 receive a very low voltage (e.g. a negative voltage). During a hold operation, first channel interface 42 may receive a low voltage or high voltage from bit line BL. This fluctuation of voltage over the bit line BL during a hold operation may be attributed to activity relating to another memory cell that shares bit line BL with transistor 41.

[29] During a write operation, second channel interface 44 may receive a low voltage and gate 40 may receive a high voltage. During writing of a logical 0, first channel interface 42 may receive a low voltage. Conversely, during writing of a logical 1, first channel interface 42 may receive a high voltage. Accordingly, as shown in Figure 7, at no point during a hold, purge, or write operation are there extreme voltage differences between any of the interfaces of the transistor. Accordingly, operation of a Floating Body Dynamic Random Access Memory FBDRAM can be accomplished with smaller scale devices that have lower tolerances.

[30] In embodiments of the present invention a very low voltage is a negative voltage in a range of -0.5V to -2.5V. In embodiments, a high voltage is a positive voltage in a range of 0.5V to 2.5V. In embodiments, a low voltage is a ground voltage that is approximately 0V.

[31] The foregoing embodiments and advantages are merely exemplary and are not to be construed as limiting the present invention. The present teaching can be readily applied to other types of apparatuses. The description of the present invention is intended to be illustrative, and not to limit the scope of the claims. Many alternatives, modifications, and variations will be apparent to those skilled in the art.